UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/811,995	03/19/2001	Matthew J. Adiletta	10559-320001/P9681	9585

20985 7590 08/18/2004

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
O BRIEN, BARRY J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/811,995	ADILETTA ET AL.	
	Examiner	Art Unit	
	Barry J. O'Brien	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2004 and 09 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-16* is/are pending in the application.

4a) Of the above claim(s) *9-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20040609*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment A as received on 6/03/04 and IDS as received on 6/09/04.

Election/Restrictions

3. Newly submitted claims 9-16 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:

4. Claims 1-7 (Group I) are drawn to a processor with the ability to chose, depending on a bit mask, bytes to be selected from multiple sources, including a general purpose register, a read transfer register, and an immediate data bus, to be loaded into an ALU for further processing. However, newly submitted claims 9-16 (Group II) are drawn to a pipelined processor with a multi-banked register file, thread switch logic, and windowed register files and transfer register stacks.

5. Inventions I and II are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the method of selecting certain source bytes in

response to a bit mask can be executed on any processor with the hardware recited in claims 1 and 5. The subcombination has separate utility such as being used as a general-purpose processor with the ability to execute instructions that can take advantage of its banked and windowed register files and stacks.

6. Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

7. Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 9-16 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Specification

8. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

9. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Rejections - 35 USC § 112

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 1-4 and 6-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

12. Claim 1 recites the limitation, "An execution unit for executing multiple context threads" on its second line. It is unclear whether this refers to threads having multiple contexts, or whether it refers to multiple contexts with each context being its own thread. For the purposes of the examination, the examiner will assume that the execution unit is capable of executing multiple threads, each thread being a separate context of some sort. Dependent claims 2-4 contain all of the limitations of their parent claim, and thus are rejected for the same reasons as above.

13. Claim 2 recites the limitation "the data" in its second line. There is insufficient antecedent basis for this limitation in the claim. See also claim 3 which contains a similar problem requiring correction.

14. Claim 6 recites the limitation, "Including a bit mask" on its third line. It is unclear how the execution of a register instruction can comprise a method step of "including a bit mask", as it appears that the register instruction actually contains the bit mask. Please clarify the claim language to more clearly define the metes and bounds of the claimed invention. See also claim 7 which contains a similar problem requiring correction.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by Portanova et al., U.S. Patent No. 4,992,934.

17. Regarding claim 1, Portanova has taught a processor, comprising:

a. An execution unit for executing multiple context threads, said execution unit comprises:

I. An arithmetic logic unit to process operands for executing threads (104 of Fig.3). Here, because a thread is defined as a sequential flow of instructions, the ALU (104 of Fig.3) inherently executes threads.

II. A multiplexor (124 of Fig.3),

III. Control logic to control the operation of the arithmetic logic unit and the multiplexor (30 of Fig.3),

IV. An immediate data bus coupled from the output of the control logic to an input of the multiplexor to provide immediate data to the arithmetic logic unit through the multiplexor (see Fig.3 and Col.14 lines 32-42),

V. A general purpose register set (74 of Fig.3) that includes a plurality of general purpose registers coupled to the input of the multiplexor

to provide register operand data to the arithmetic logic unit through the multiplexor (see Fig.3 and Col.14 lines 8-17),

VI A read transfer register (232 of Fig.3) coupled to the input of the multiplexor to provide operand data from a memory device (see Col.21 lines 50-55),

VII. Wherein execution of a register instruction causes data from one or more input sources connected to the multiplexor to be transferred through the multiplexor into the arithmetic logic unit and causes data to be transferred through the arithmetic logic unit to one of the general purpose registers (100 of Fig.3, as well as Col.14 line 52 – Col.15 line 43).

18. Regarding claim 5, Portanova has taught a method for executing multiple context threads, comprising:

a. Processing operands for an executing context thread of multiple context threads through a multiplexor (124 of Fig.3) and an arithmetic logic unit (104 of Fig.3). Here, because the RISC processor executes branch instructions that allow one sequential flow of instructions to branch to another context (new sequential flow of instructions) (see Col.1 lines 24-30 and Col.3 lines 24-30), and further because a thread is defined as a sequential flow of instructions, the ALU (104 of Fig.3) inherently executes threads.

b. Operating control logic (30 of Fig.3) connected to the arithmetic logic unit and the multiplexor (see Fig.3),

c. Providing immediate data on an immediate data bus coupled from the output of the control logic to an input of the multiplexor (see Fig.3 and Col.14 lines 32-42),

d. Providing operand data to the arithmetic logic unit from a general purpose register (78 of Fig.3) coupled to the input of the multiplexor (see Fig.3 and Col.14 lines 8-17),

e. Providing operand data from a memory device through a read transfer register (232 of Fig.3) coupled to the input of the multiplexor (see Fig.3 and Col.21 lines 50-55),

f. Executing a register instruction to cause data from one or more input sources connected to the multiplexor to be transferred through the multiplexor into the arithmetic logic unit and to cause data to be transferred through the arithmetic logic unit to one of the registers (100 of Fig.3, as well as Col.14 line 52 – Col.15 line 43).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Portanova et al., U.S. Patent No. 4,992,934, as applied to claim 1 above, and further in view of

Patterson et al., *Computer Organization and Design: The Hardware/Software Interface* (hereinafter Patterson).

21. Regarding claim 4, Portanova has taught the processor of claim 1, but has not explicitly taught wherein the processor further comprises:

a. A bypass bus coupled from the output of the arithmetic logic unit to an input of the multiplexor,

b. Control logic to control the execution of a series of pipelined instructions wherein each pipelined instruction may specify a read part and a write part, where the read part of one pipelined instruction specifies a read address that is the same as a write address of the write part of another pipelined instruction causing the data being written by the write part to be available to the read part in the same processor cycle.

22. However, Patterson has taught a bypass bus which connects the output of an ALU to the input of the multiplexer (see part b of Fig. 6.38). Patterson has also taught control logic (see Forwarding Unit of Fig. 6.38) which allows data that is written in one pipelined instruction to be forwarded to another instruction attempting to read that data (see Fig. 6.37) so that data hazards can be resolved without stalling the pipeline (see p.480). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Portanova to include this data forwarding logic which allows the processor to forward data from one pipeline instruction to another in order to resolve data hazards and prevent the processor from stalling.

23. Claims 2-3 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Portanova et al., U.S. Patent No. 4,992,934 as applied to claim 1 above, and further in view of the *Intel IA-64 Application Developer's Architecture Guide* (hereinafter Intel).

24. Regarding claims 2 and 6, taking claim 2 as exemplary, Portanova has taught the processor of claim 1, but has not explicitly taught wherein the register instruction includes a bit mask specifying which one or more bytes of the data are affected and causing the bytes of the data specified by the bit mask to be loaded into the arithmetic logic unit from the immediate data bus and the bytes of the data not specified to be loaded from the read transfer register.

25. However, the Intel has taught a "mix1" instruction, which based on a bit mask selects certain bytes of data held in a first source to be loaded into a destination register, and the remaining bytes specified by the mask to be loaded from data held in a second source (see Sec. 4.6.3 of p.4-31, p.7-116 – 7-118 and p.C-21). Here, the bit mask is the opcode and the extension fields which modify the opcode in order to determine which sources, and which bytes within the sources, are selected to be loaded. One of ordinary skill in the art would have recognized that having multimedia instructions expands the functionality of a processor in a desirable way as well as improve performance (see Sec. 2.3 of p.2-2 and Sec. 4.6 of p.4-29). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Portanova to include a mix1 instruction containing a bit mask which selects bytes from a first source, the immediate data bus (see Portanova, Fig.3 and Col.14 lines 32-42), and selects the remaining bytes from a second source, the read transfer register (see Portanova, 232 of Fig.3) so that the functionality of

the processor can be expanded in a useful and efficient manner and performance can be increased.

26. Claim 6 is nearly identical to claim 2, differing in its parent claim, but encompassing the same scope as claim 2. Therefore, claim 6 is rejected for the same reasons as claim 2.

27. Regarding claims 3 and 7, taking claim 3 as exemplary, Portanova has taught the processor of claim 1, but has not explicitly taught wherein the register instruction includes a bit mask specifying which one or more bytes of the data are affected and causing the bytes of the data specified by the bit mask to be loaded into the arithmetic logic unit from the immediate data bus and the bytes of the data not specified to be loaded from the general purpose register.

28. However, Intel has taught a "mix1" instruction, which based on a bit mask selects certain bytes of data held in a first source to be loaded into a destination register, and the remaining bytes specified by the mask to be loaded from data held in a second source (see Sec. 4.6.3 of p.4-31, p.7-116 – 7-118 and p.C-21). Here, the bit mask is the opcode and the extension fields which modify the opcode in order to determine which sources, and which bytes within the sources, are selected to be loaded. One of ordinary skill in the art would have recognized that having multimedia instructions expands the functionality of a processor in a desirable way as well as improve performance (see Sec. 2.3 of p.2-2 and Sec. 4.6 of p.4-29). Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Portanova to include a mix1 instruction containing a bit mask which selects bytes from a first source, the immediate data bus (see Portanova, Fig.3 and Col.14 lines 32-42), and selects the remaining bytes from a second source, the

general purpose register (see Portanova, 78 of Fig.3) so that the functionality of the processor can be expanded in a useful and efficient manner and performance can be increased.

29. Claim 7 is nearly identical to claim 3, differing in its parent claim, but encompassing the same scope as claim 3. Therefore, claim 7 is rejected for the same reasons as claim 3.

Response to Arguments

30. Applicant's arguments filed 6/03/04 have been fully considered but they are not persuasive.

31. On p.8 of the present amendment filed 6/03/04, the Applicant argues with respect to claim 1:

> *"Claim 1 recites "an execution unit for executing multiple context threads." At least this quoted claim feature is neither disclosed nor suggested in Portanova. Accordingly, claim 1 is not anticipated by Portanova."*

32. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Furthermore, the prior art of reference has, in fact, taught such a limitation, as shown above in paragraph 12, and thus claim 1 stands rejected in view of Portanova.

33. On p.8 of the present amendment filed 6/03/04, the Applicant argues with respect to claim 5:

"Claim 5 recites "processing operands for an executing context thread of multiple context threads through a multiplexor and an arithmetic logic unit." At least this quoted claim feature is neither disclosed nor suggested in Portanova. Accordingly, claim 5 is not anticipated by Portanova."

34. Applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Furthermore, the prior art of reference has, in fact, taught such a limitation, as shown above in paragraph 13, and thus claim 5 stands rejected in view of Portanova.

Conclusion

35. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

36. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection

of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

37. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

38. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
8/9/2004

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100